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PATENT APPLICATION

HOT-SWAP PROTECTION CIRCUIT

Inventor: Sam Seii Ochi, a citizen of The United States, residing at
19920 Saraglen Court
Saratoga, CA 95070

Assignee: IXYS Corporation
3540 Bassett Street
Santa Clara, CA 95054
A California corporation

Entity: Small business concern

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400

HOT-SWAP PROTECTION CIRCUIT

CROSS-REFERENCES TO RELATED APPLICATIONS

[01] The present application is related to and claims priority from U.S. Provisional Application No. 60/258,004, filed December 22, 2000.

STATEMENT AS TO RIGHTS TO INVENTIONS MADE UNDER FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

[02] NOT APPLICABLE

REFERENCE TO A "SEQUENCE LISTING," A TABLE, OR A COMPUTER PROGRAM LISTING APPENDIX SUBMITTED ON A COMPACT DISK.

[03] NOT APPLICABLE

BACKGROUND OF THE INVENTION

[04] The present invention relates generally to integrated circuits. More particularly, the invention relates to a method and circuitry for hot-swap protection circuits.

[05] A hot swap operation is an insertion action or a removal action of a device while the system using it is receiving power, coupling the power from the system to the device. Such an operation can cause external capacitors to draw currents high enough to disturb system operations or even cause permanent damage to either or both the device and the system.

[06] Hot-swap protection circuits enable electronic circuits to be connected to each other and disconnected from each other while powered. Hot-swap protection circuits are required in many applications where it is not practical to shut down an electronic system while replacing or adding circuit boards to it. Such protection circuits, or systems, are used in telephone switching hubs, corporate network server hubs, and in laptop or desktop computers with PCMCIA connectors. All of the examples require connection or disconnection under power and so on.

[07] Conventional hot-swap protection circuits employ connectors with at least one set of sensor pins, which are a set of extra long and extra short pins, connected to voltage detectors. These sensor pins allow immediate detection of connection and/or disconnection by sensing the presence and/or absence of the applied voltage. It is well known that a single set of

sensor pins—whether at the top, middle, or bottom—might not be enough to detect a hot-swap event.

[08] For the best reliability, it is often necessary to use two sets of sensor pins, one set at the top and one set at the bottom of a hot-swappable card. Adding additional sets of sensor pins increase reliability, but increases costs to the overall system. Additionally, conventional hot-swap protection systems using sensor pins do not always detect the application or removal of power to a system.

BRIEF SUMMARY OF THE INVENTION

[09] The present invention provides a method and circuitry for hot swap operations. Application of power from a source of power is detected by first circuitry. A switch couples the power to the device in a gradual manner in responsive to the first circuitry. Circuitry is provided which detects an overcurrent condition in which the current draw by the device exceeds a predetermined level. The switch decouples the device from the power responsive to the circuitry. Circuitry is provided detects events in which power is removed momentarily, as occurs in a ground-fault condition, or permanently as in a disconnect event, and in response thereto a signal is produced indicative of the occurrence. Circuitry, which is responsive to noise in the power, is operatively coupled with the switch which varies its conductance in response to the detected noise.

[10] Embodiments of the present invention achieve their purposes and benefits in the context of known circuit and process technology and known techniques in the electronic and process arts. Further understanding, however, of the nature, features, and advantages of the present invention is realized by reference to the latter portions of the specification, accompanying drawings, and appended claims. Other features and advantages of the present invention will become apparent upon consideration of the following detailed description, accompanying drawings, and appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[11] Fig. 1 is a simplified high-level block diagram of an electronic hot-swap protection circuit, according to one embodiment of the present invention;

[12] Fig. 2 is a simplified high-level schematic diagram of the hot-swap protection circuit of Fig. 1, according to one embodiment of the present invention;

[13] Fig. 3 is a simplified high-level schematic diagram of the hot-swap protection circuit of Fig. 1, according to another embodiment of the present invention;

[14] Fig. 4 is a simplified high-level block diagram of an electronic hot-swap protection circuit, according to another embodiment of the present invention;

[15] Fig. 5 is a simplified high-level schematic diagram of the hot-swap protection circuit of Fig. 4, according to one embodiment of the present invention;

[16] Fig. 6 is a simplified high-level schematic diagram of the hot-swap protection circuit of Fig. 5, according to another embodiment of the present invention;

[17] Fig. 7 is a simplified high-level schematic diagram of the hot-swap protection circuit of Fig. 4, according to another embodiment of the present invention; and

[18] Fig. 8 is a simplified high-level schematic diagram of the hot-swap protection circuit of Fig. 7, according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[19] Fig. 1 is a simplified high-level block diagram of an electronic hot-swap protection circuit 100, according to one embodiment of the present invention. Fig. 1 shows a detector 102 coupled in series, via a connector 105, to an electrical power source 107. Detector 102 also couples in series to a fast-disconnect, slow-reconnect switch 110. Switch 110 couples in series along a power supply conductor between a load 112 (circuit to be protected, target circuit, device, etc.) and power source 107. Detector 102 includes an overcurrent detector module 115 and a control circuit 117. Detector module 115 is series-coupled between switch 110 and a first terminal of connector 105. Control circuit 117 is coupled to a second terminal of connector 105. Detector module 115 includes an output that feeds into control circuit 117.

[20] In this specific embodiment, detector module 115 and switch 110 couple to the positive terminal of power supply 107, and control circuit 117 couples to the negative terminal of power supply 107. Alternatively, detector module 115 and switch 110 can be located on the negative terminal of power source 107, with appropriate modifications to the circuitry.

[21] In operation, detector 102 detects whether load 112 is hot-swapped in, i.e., reconnected to power source 107. When detector 102 detects a reconnect event, it outputs a hot-swap occurrence indication, or "indication," or "control signal." More specifically, detector 102 sends a hot-swap occurrence indication, i.e., a reconnect control signal, to switch 110 instructing it to close, i.e., turn on, in accordance with the invention.

Hot-Swap Occurrence Indication

[22] In this and in other embodiments of the present invention, the hot-swap occurrence indication can serve other functions and will depend on the specific application. For example, the indication can be coupled to drive an LED to notify a user of the hot-swap occurrence. The indication can also be coupled to a controller or microprocessor in the form of an interrupt signal, for example, so that appropriate processing can be performed.

[23] In this specific embodiment, the reconnect control signal is produced by control circuit 117. Also, in this specific embodiment, switch 110 opens quickly but closes slowly. Upon reconnection, the conductivity of switch 110 gradually increases to a fully conductive state, i.e., non-binary change of state that is gradual as opposed to discrete.

[24] Upon detection of a reconnect event, detector module 115 produces a signal indicative of a reconnect event. The signal feeds to control circuit 117 which then produces an indication signal and a control signal. The control signal feeds to switch 110. As will be explained below, the control signal is of a nature as to cause switch 110 to gradually increase its conductance (i.e., gradually decrease its resistance).

[25] A reconnect event is typified by a detection of a presence of voltage following the absence of current. The term "reconnect" implies the load 112 was previously connected. However, it is possible that a load might never have been connected to the powered system, in which case the term "connect" is more appropriate. For purposes of this disclosure, however, the terms "reconnect" and "connect" are used interchangeably, since both situations are the same from the point of view of a hot swap operation.

[26] Fig. 2 is a simplified high-level schematic diagram of a hot-swap protection circuit 100 in accordance with an illustrative embodiment of the present invention. Hot-swap protection circuit 100 is implemented with commonly available integrated circuits including discrete-active and -passive components (see Figs. 6 and 8, for example). Hot-swap protection circuit 100 includes detector 102 and switch 110, both of which are located on the negative terminal of power source 107. Alternatively, in other embodiments, detector 102 and switch 110 can be located on the positive terminal of power source 107 (as in Fig. 1), with appropriate modifications to the circuitry.

[27] In this specific embodiment, load 112 couples in parallel to a capacitor 120. Fig. 2 shows a schematic of the switch. Typically, the switch 110 is a MOSFET device such as the one shown in Fig. 2 having a part number BUK456. Of course, other commercially available switches can be substituted; e.g., Fig. 6 shows a FET having a part number IRF2807.

[28] Detector module 115 includes an operational amplifier 127, or op-amp 127, configured to output a hot-swap occurrence indication, e.g., a reconnect control signal. The non-inverting input of op-amp 127 couples to switch 110 and inverting input of op-amp 127 couples to the negative terminal of power source 107 via a voltage source 130. A resistor 132 couples between the inverting and non-inverting inputs of op-amp 127. In this specific embodiment, for example, op-amp 127 is implemented with an integrated circuit operational amplifier identified by the part number MC33174. Other commercially available op-amps or similar devices can be used.

[29] Control circuit 117 includes a diode 135, resistor 137, and a Zenor diode 140 coupled in series between the positive and negative terminals of power source 107. A resistor 142 and a capacitor 144 couple in parallel between the positive and negative terminals of power source 107. A resistor 147 and a capacitor 150 couple in series with capacitor 144. A transistor 152 couples between a gate switch 110 (node V_{GATE}) and the negative terminal of power source 107. Transistor 152 has a gate coupled to the output of op-amp 217. Node V_{GATE} couples control circuit 117 to switch 110.

[30] In operation, generally, hot-swap protection circuit 100 of Fig. 2 functions to enable the soft (gradual) application of the voltage at node V_{IN} to the load 112. This soft application reduces the stress to the components within load 112 as well as to capacitor 120. Such stress can cause physical damage to these components. For example, if an instantaneous voltage is applied across load 112 or capacitor 120, it is theoretically possible to cause infinite current flow through load 112 or capacitor 120. This can either degrade them or immediately cause them to explode, causing physical damage and possible destruction.

[31] Suppose that after load 112 is reconnected for a sufficient amount of time such that the voltage at node V_{OUT} settles to a voltage close that at node V_{IN}, and a steady state current flow through load 112 is established. The difference between voltages at nodes V_{OUT} and V_{IN} is simply the load current through load 112 times the sum of the resistances of resistor 132 and a resistance Rdson of switch 110 in the conducting state.

Operation of Detector 102 upon reconnection

[32] Upon reconnection, hot-swap protection circuit 100 enables a soft turn-on of switch 110 through resistor 147. The soft start sequence is as follows. First, assume that all of the capacitors in control circuit 117, as well as capacitor 120 across the load 112, are discharged so that the potential at node V_{IN} at connector 105 is at zero potential. Second, power source 107 couples to detector module 102 via connector 105. The application of the voltage at

node V_{IN} at the output of the connector 105 causes the presence of a voltage E_{IN}, i.e., voltage of power source 107 at node N. Capacitor 144 then charges through resistor 137 to 12V, the voltage of which is determined and limited by Zenor diode 140. In other embodiments, Zenor diode 140 can have other values. During this time, the voltage at node V_{GATE} ramps up from zero potential through resistor 147, implementing a "soft" or slow turn-on of switch 110. The voltage at node V_{OUT} then quickly ramps up from a zero potential to the voltage at node V_{IN}. The ramp-up rate is determined by the turn-on rate of switch 110 and the size of capacitor 120 across the load 112.

[33] Fig. 3 is a simplified high-level schematic diagram of a hot-swap protection circuit 100 in accordance with another illustrative embodiment of the invention. Hot-swap protection circuit 100 of Fig. 3 is similar to that of Fig. 2. In the embodiment shown in Fig. 3, detector 102 includes circuit 160.

Circuit 160

[34] Circuit 160 includes an operational amplifier 162, or op-amp 162. An output of op-amp 162 couples to the gate of switch 110, or node V_{GATE}, via a resistor 165. Node V_{GATE} couples between resistor 147 and capacitor 150 via a diode 167. A bias voltage source 170 couples in parallel to capacitor 150. In this particular embodiment, bias voltage source 170 is a voltage divider. Bias voltage source 170 includes a resistor 172 and a resistor 175. An inverting input of op-amp 162 couples between resistors 172 and 175 via a resistor 177 and to node V_{GROUND} via a capacitor 180.

[35] In the specific illustrative embodiments of Figs. 2, 3, 5, 6, 7, and 8, V_{GROUND} located at the positive terminal of power source 107 because the protection circuit of these specific embodiments operates in the negative voltage range. The specific voltage range in which the protection circuit operates will depend on the specific application. For example, the operating voltage range can also be in both the negative and positive voltage ranges. In some embodiments, the operating voltage range can only positive voltage ranges, for example, where $V_{GROUND} = 0V$.

Operation of Circuit 160

[36] Circuit 160 protects load 112 from noise that might be present in power source 107. Circuit 160 operates in conjunction with switch 110 to effectively function as a low pass filter of the power from power source 107, thus reducing the effects of noise present in the power. The op-amp 162 is configured as a voltage follower. Noise from power source 107 will

propagate through network 170 to the inverted input 13 of op-amp 162 through the network of resistor 177 and capacitor 180. The noise components will cause a differential input to appear at the input of op-amp 162. The resulting output of op-amp 162 will drive switch 110 to alter its conductivity as a function of the noise. This in turn alters the current flow to load 112. Consequently, the power delivered to load 112 will be effectively low-pass filtered by the switch. Thus, by altering the conductivity of the switch 110 in response to noise present in the power, the noise components in the power delivered to the load 112 can be reduced.

Operation of Overcurrent Detector Module 115 (load connected)

[37] The following description assumes that load 112 has been connected to power source 107 through switch 110, which is on, and through overcurrent detector module 115. As long as the voltage drop across resistor 132 is less than voltage source 130, e.g., Vcl=100mV, the output of op-amp 127 will be low, or at the voltage at node V_{IN}. This keeps transistor 152 of control circuit 117 off and node V_{GATE} high which keeps switch 110 on.

[38] An overcurrent condition is one where load 112 demands a much higher than normally expected current. For example, suppose that the current is so high that the voltage drop across resistor 132 is greater than 100mV. This causes the non-inverting input of op-amp 127 to become more positive than its inverting input. Note that the voltage differential across the non-inverting and the inverting inputs occurs when a detected overcurrent condition is detected. In this specific example, an overcurrent is detected when the voltage drop across resistor 132 is greater than 100mV, or if greater than 10 amps of current flow through resistor 132. The threshold current which defines an overcurrent condition can be predetermined by setting voltage level of voltage source 130 accordingly.

[39] Upon detection of an overcurrent condition, overcurrent detector module 115 causes the output of op-amp 127 to go high, or +12V. This turns on transistor 152 to discharge capacitor 150 to the voltage at node V_{IN}. This discharged of capacitor 150, Vc1=~0V, causes switch 110 in switch 110 to turn off which results the disconnection of load 112. After switch 110 turns off, the output of op-amp 127 drops back down to 0V, or the voltage at node V_{IN}, because the current through resistor 132 is cut off. Also, capacitor 150 begins to recharge.

[40] The same logical high signal with respect to node V_{IN} (which is available from op-amp 127) becomes an indication output. This indication output indicates an overcurrent fault shut down.

[41] Fig. 4 is a simplified high-level block diagram of an electronic hot-swap protection circuit 100, according to another embodiment of the present invention. Hot-swap protection circuit 100 Fig. 4 is configured similarly to that of Fig. 1 except that circuit 100 of Fig. 4 includes a detector 181 that detects whether load 112 is hot-swapped out, i.e., disconnected from power source 107. In this specific embodiment, detector 102 couples in parallel to a switch 110. Switch 110 couples in series to a terminal of power source 107 via connector 105 and to load 112.

[42] When detector 102 detects a disconnect event, it outputs a hot-swap occurrence indication, or "indication," or "control signal." More specifically, detector 102 sends a hot-swap occurrence indication, i.e., a disconnect control signal, to switch 110 causing it to open, i.e., turn off. Switch 110 opens quickly.

Hot-Swap Occurrence Indication

[43] As stated above, the hot-swap occurrence indication can serve other functions which depend on the specific application. For example, the indication can be coupled to drive an LED to notify a user of the hot-swap occurrence. The indication can also send a signal to a controller or microprocessor as an interrupt signal to perform appropriate processing in the occurrence of a disconnect. During a disconnect event in a storage device, for example, certain cleanup operations can be performed before the drive loses all of its power.

[44] Fig. 5 is a simplified high-level schematic diagram of a hot-swap protection circuit 100, which in some embodiments of the present invention, can be used to implement the hot-swap protection circuit of Fig. 4. Like hot-swap protection circuit 100 of Fig. 4, that of Fig. 5 is implemented with commonly available integrated circuits including discrete-active and -passive components.

[45] Hot-swap protection circuit 100 of Fig. 5 includes detector 181 and switch 110, both of which are located on the negative terminal of power source 107. Alternatively, in other embodiments, detector 181 and switch 110 can be located on the positive polarity conductor of the power source 107 (as in Fig. 4), with appropriate modifications to the circuitry.

[46] In this specific embodiment, detector 181 of Fig. 5 includes the same elements and configuration as that of Fig. 2 with a few exceptions. Detector 181 of Fig. 5 includes a ground-fault protection circuit 185 in place of overcurrent protection circuit 115 of Fig. 2.

[47] Upon detection of a disconnect event, detector module 185 sends an output indication, or "signal," to control circuit 117. Accordingly, if the signal is triggered by a disconnect

event, control circuit 117 sends a disconnect control signal to switch 110 instructing it to open.

[48] Switch 110 couples between the non-inverting input and the inverting input of an op-amp 187 via a voltage source 192.

Operation of Detector 181 upon disconnection

[49] In operation, hot-swap protection circuit 100 of Fig. 5, functions as a load-disconnect protection circuit. Prior to disconnection, assuming that load 112 is powered normally and operational. The voltage at node V_{OUT} is approximately equal to that at node V_{IN}, less the voltage drop across switch 110. The voltage drop across switch 110 is such that the voltage at node V_{OUT} is more positive than that at node V_{IN}, because current is being supplied to load 112 through switch 110 from node V_{IN}. Op-amp 187 of detector 181 connects across switch 110. The non-inverting input of op-amp 187 couples to a voltage source Vos 192. The value of voltage source 192 is approximately −10mV and can vary depending on the specific application. The -10mV ensures that the output of op-amp 187 is low relative to the voltage at node V_{IN}, regardless of the current flow of load 112, or regardless of any finite built-in offset voltages of op-amp 187 (assuming that the input offset voltage of op-amp 187 < 10mV). This keeps transistor 152 off so that node V_{GATE} is charged to 12V, keeping switch 112 on.

Operation of Ground-Fault Protection Circuit 185 (load gets disconnected)

[50] The following description assumes that at some time T1 connector 105 disconnects due to a ground fault-condition. Because there are no capacitors connected between nodes V_{GROUND} and V_{IN}, the voltage at node V_{IN} has the tendency to move towards the voltage at node V_{GROUND}. However, this does not happen because the charge on capacitor 120, which was initially charged to the voltage at node V_{OUT}. Capacitor 120 sustains a current flow from node V_{OUT} to node V_{IN}. As long as there is available charge in capacitor 120 to sustain the current needed by detector 181, it will function properly.

[51] In operation, detector 181 recognizes immediately that the voltage across switch 110 is now reversed, i.e., the voltage at node V_{OUT} is more positive than that at node V_{IN}. The output of op-amp 187 goes high to turn on transistor 152, which in turn discharges capacitor 150. This causes switch 110 in switch 110 to turn off which results the disconnection of load 112. This also stops the discharge of capacitor 120 by the detector 181.

[52] In some embodiments of the invention, because the logical high signal that op-amp 187 outputs also functions as a hot-swap occurrence indication, the indication can be sent to other circuits, e.g., LED, controller, microprocessor, etc., for other purposes.

[53] This circuit technique detects the presence (indication low) or absence (indication high) from detector 181, and represents an automatic ground fault detection without the need for separate ground sense pins as needed in the prior art.

[54] It is to be understood that this specific implementation as depicted and described herein is for illustrative purposes only and should not limit the scope of the claims herein, and that alternative circuit implementations exist for the same functionality. For example, any IC chip, proprietary or otherwise, can be used to implements the circuits described herein.

[55] The foregoing circuits can be readily implemented using any of a number of commercially available integrated circuit devices. For example, Fig. 6 illustrates how the hot-swap protection circuit according to the present invention as shown in Fig. 5 can be provided using conventional hot-swap IC devices. Attached as Appendix A is a data sheet for the IC device. Following is a description of the pin outs of the chip:

Pin 1 (INV) provides an invert input function. The invert input controls GSNSin's polarity. When invert input is high compared to AGND, then GSNSin low indicates an insertion/removal event. When invert input is low, then GSNSin high indicates an insertion/removal event.

Pin 15 (GSNSin) provides a ground sense input. The INV pin controls the polarity sense of this input. A 3uA internal pull-up current source causes logic high when there is no connection at this pin. With INV low or connected to AGND, a GSNSin low (or connected to AGND) will keep RSTout and GATE low, and the external power switch, Q1, off. A disconnected GSNSin pin or when Vcc is applied to it will allow normal operation.

Pin 2 (VCCin) is the supply voltage positive power-supply voltage input.

Pin 3 (SHNToff) is the shunt off pin. This pin serves to control the enabling of the shunt circuit. When the pin is high compared to AGND, then the shunt regulator is in off position. A low level at this pin activates the shunt regulator.

Pin 4 (CAPin) is an active lowpass filter capacitor input. The output of the power active filter tracks this pin. Adding an external RC network matching the input noise with respect to the 3db point of the filter could reduce the noise to a minimum.

Pin 5 (VDROP) is an active filter offset voltage pin. This pin sets the drop out MOSFET voltage across the active filter.

Pin 6 (SLOPE) is a slope input pin. This input controls the current slope during power up and controls inrush currents. Adding external capacitors to this pin allow regulation and adjustment of the rate of the current slope.

Pin 7 (OFFTM) is the off-time pin. The OFFTM pin sets the delay time between powerdown and restart of IXHQ100. Delay time can be increased by adding external capacitors to this pin.

Pin 8 (AGND) is the ground pin. This pin provides a system zero reference pin.

Pin 9 (VDDout) is the regulator output voltage pin. The regulator output voltage provides current to drive the external circuits with respect to AGND.

Pin 10 (VCL) is the vercurrent threshold bias voltage pin. This pin sets the overcurrent threshold bias voltage.

Pin 11 (SOURCE) is the current input sensor pin. This serves as the input pin for sensing current through the power device with respect to AGND.

Pin 12 (GATE) in the output pin. This is control voltage pin for driving an external MOSFET.

Pin 13 (OUTsns) is the out sensor signal pin. This signal pin senses the output voltage of the circuit.

Pin 14 (RSTout) is the output reset pin. A low at this pin indicates detection of an insert/removal event or overcurrent detection.

Pin 16 (NC) N/A Not Connected

[56]

[57] Fig. 7 is a simplified high-level schematic diagram of a hot-swap protection circuit 100, which in some embodiments of the present invention, can be used to implement the hot-swap protection circuit of Fig. 4. Hot-swap protection circuit 100 of Fig. 7 is similar to that of Fig. 5 except that it includes a filter 160. In this particular embodiment, filter 160 is an active filter. Also, filter 160 of this specific embodiment is implemented with commonly available integrated circuits and discrete active and passive components.

[58] Filter 160 of Fig. 7 includes the same elements and is configured similarly to that of Fig. 3 except that the non-inverting input of op-amp 162 couples to the drain of switch 110 as well as to the inverting input of op-amp 187.

[59] Fig. 8 further illustrates how the hot-swap protection circuit according to the present invention as shown in Fig. 5 can be provided using conventional hot-swap IC devices. The circuit shown in Fig. 8 uses the IC device described in the data sheet of Appendix A that can be used to implement the hot-swap protection circuit of Fig. 7. In addition, Figure 1 in the data sheet of Appendix A shows a configuration which implements a hot swap protection circuit according to the present invention as shown in Fig. 3.

[60] Other similar commercially available IC devices can be used to implement the hot swap protection circuits disclosed herein. For example, Linear Technology sells a line of hot

swap controllers such as part nos. LT1640AH and LT1640AL. Texas Instruments Incorporated sells a line of hot swap IC devices such as TPS2320 and TPS2321. Maxim Integrated Products sells IC devices such as the MAX5904 which can be used. The disclosed hot swap protection circuitry according to the present invention can be made using such IC devices in conjunction with appropriate external components.

[61] Specific embodiments of the present invention are presented above for purposes of illustration and description. The full description will enable others skilled in the art to best utilize and practice the invention in various embodiments and with various modifications suited to particular uses. After reading and understanding the present disclosure, many modifications, variations, alternatives, and equivalents will be apparent to a person skilled in the art. The foregoing, therefore, is not intended to be exhaustive or to limit the invention to the specific embodiments described. The claimed invention is intended to be accorded the widest scope consistent with the principles and novel features disclosed herein, and as recited in the following claims.

HOT-SWAP PROTECTION CIRCUIT

APPENDIX A

IXYS

IXHQ 100PI
IXHQ 100SI

Negative Voltage Hot Swap Controller with Active Power Filter

Features

- **Live Insertion and Removal Power Manager**
- **Adjustable Power-on slew rate**
- **Autodetect of Load Open Circuit or -VIN Disconnection**
- **C ntrolled Time-Delay**
- **Operates from -9 V to External MOSFET Voltage Limit**
- **Fault Indication Output (microprocessor reset).**
- **B ard Insertion/Removal Detector Input**
- **Protection During Turn-On**
- **Low frequency Power Active Filter**
- **Adjustable Electronic Circuit Breaker**
- **V_{in} undervoltage with GSNSin input**

Applications

- **Arcless card insertion and removal**
- **Central Office Switching Hardware**
- **Circuit Boards From -48 V Distributed Power Supplies**
- **Circuit Board Power Manager and Noise Filter**
- **Circuit Board Hot Swap Protector and Manager**
- **Electronic Circuit Breaker**
- **Wireless Local Loop Antennas**
- **Cable TV Antenna**

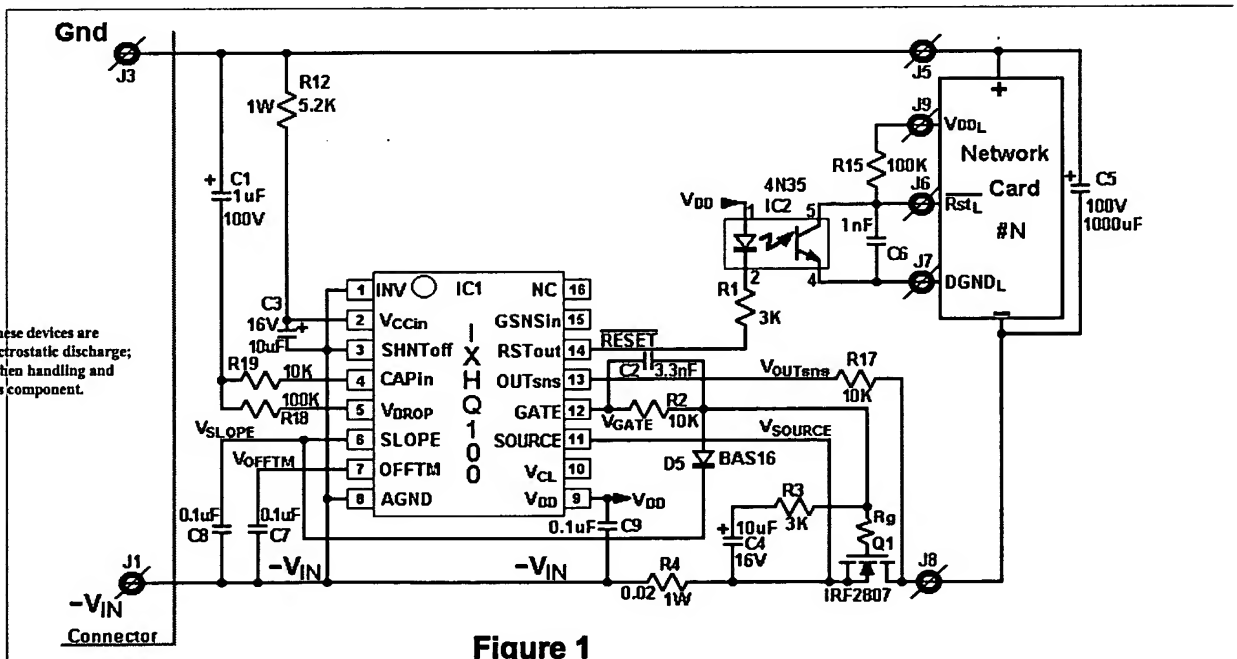
Description

The IXHQ100 is a live insertion and removal hot swap controller with a built-in power noise filter. It incorporates all the active circuitry necessary to protect circuit boards during live insertion or removal (insertion or removal when the system power is active). Additionally, the IXHQ100 incorporates two unique features: power active filter for powerline noise suppression and power auto-disconnect detector which eliminates the need of additional staggered pins.

The IXHQ100 shunt regulator ensures a wide operating voltage range (with the external MOSFET breakdown voltage as limit). The active power filter reduces power source output impedance, producing "clean" load power. The IXHQ100 allows continuous load current rise adjustments, presettable maximum current limits, and user selectable fault indication turn off times for resetting µPs and other synchronous board level systems. For added flexibility, GSNSin pin is available to implement either circuit board insertion/removal detection or ground detection.

US Patents Pending.

Typical Application with Auto-Disconnect Detector



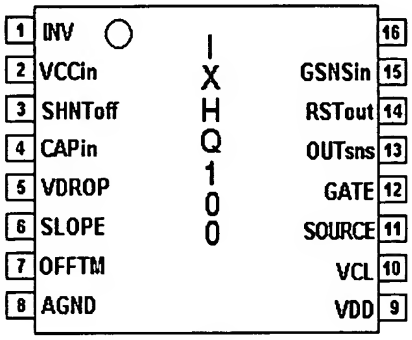
CAUTION: These devices are sensitvie to electrostatic discharge; take caution when handling and assembling this component.

Figure 1

Abs lute Maximum Ratings

Symb l	Definition	Max. Rating
V_{CC}-V_{AGND}	Voltage applied V_{CCin} to AGND	Shunt Off: -0.3 V to 16 V
	Shunt On:	-0.3 V to 14 V
	Shunt On for 10 seconds	14V to 16 V
	All other pins except V_{DC}	-0.3 V to V_{CCin} + 0.3 V
I_{VDD}	V_{DD} Load Current	60 mA
T_{JM}	Maximum Junction Temperature	125 °C
T_{J0}	Operating Temperature Range	-40 °C to 85 °C
T_{stg}	Storage Temperature Range	-40 °C to 150 °C
I_{DD}	Supply Current with Shunt On	25 mA

Pin Description



Electrical Characteristics

Unless otherwise noted, T_A = 25 °C; $-V_{IN}$= 48 V, AGND connected to $-V_{IN}$, $V_{SHUNToff}$ = 5 V, V_{CC} = 12 V, V_{GSNSin} = 12 V. All voltage measurements with respect to AGND. IXHQ100 configured as described in *Test Conditions*.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC}	Supply current	V_{CC}=12 V, $V_{SHUNToff}$ = V_{CC}, all outputs unloaded.		2	3	mA
$V_{CCSHUNT}$	V_{CC} shunt regulation voltage	I_{CC} forced to 10 mA when shunt is off	12	13.8	16	V
$V_{THSHUNToff}$	SHUNToff input threshold voltage	V_{CC} = 15 V, monitor RST_{OUT}	1	1.5	2	V
$I_{SHUNToff}$	SHUNToff input bias current		-1	0	1	µA
V_{THINV}	INV input threshold voltage	V_{CC} = 12 V, monitor RST_{OUT}	6	8	10	V
R_{INV}	INV input resistance		70	130	180	KΩ
V_{THGSNS}	GSNS sense input threshold voltage	V_{CC} = 12 V, monitor RST_{OUT}	4.5	5.8	6	V
I_{GSNSin}	GSNSin input bias current		-2.6	-2.3	-2	µA
I_{CAPin}	CAPin input bias current		-1	0	1	µA
V_{VDROP}	Active filter offset voltage		0.7	0.9	1.1	V
R_{VDROP}	V_{DROP} input resistance		50	70	90	KΩ
I_{SLOPE}	SLOPE capacitor charging current	V_{OFFTM} = 5 V, $V_{GSOURCE}$ = 0 V V_{CAPin}= 5 V	70	85	110	mA
$R_{SLOPEDCHG}$	SLOPE capacitor discharge resistance	V_{DROP} = 5 V, IVT = V_{CC} V_{SOURCE} = 0 V, V_{CAPin}= 5 V		90	200	Ω
I_{OFFTM}	OFFTM capacitor charging current	V_{DROP} = 5 V, V_{SOURCE} = 0 V V_{CAPin}= 5 V	80	100	120	mA
$R_{OFFTMCHG}$	OFFTM capacitor discharge resistance			111	200	Ω
$V_{THOFFTM}$	OFFTM input threshold voltage	OFFTM input voltage when SLOPE input voltage starts its ramp	3.8	4.5	5.5	V
V_{CL}	Overcurrent threshold bias voltage		90	125	150	mV

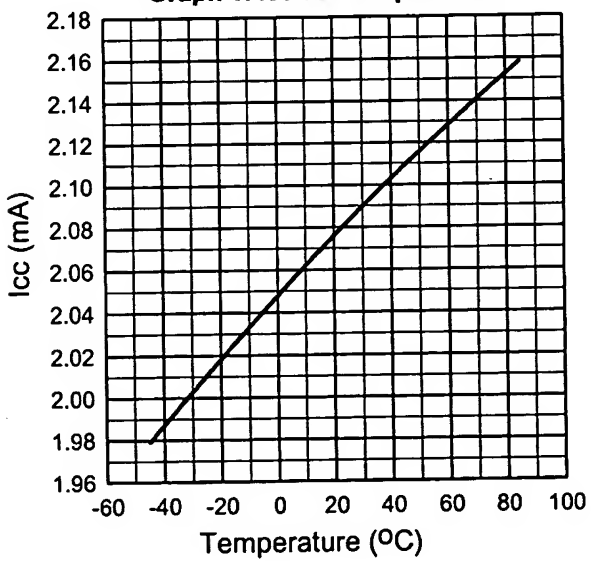
Electrical Characteristics (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
R_{VCL}	VCL bias resistance		4	6	10	kΩ
t_{OC}	Overcurrent detection to GATE output delay	V_{CAPin} = 0 V; V_{OUTsns} = 5 V V_{SOURCE} input is a step at t = 0s from 0 V to 200 mV		20	30	ms
dv_{GATE}/dt	GATE output slew rate	C_{SLOPE}= 100 nF	0.5	0.8	1.1	V/ms
V_{GATE}	Maximum GATE output voltage	V_{CAPin} = 0 V; R_{load} = 10 KΩ V_{OUTsns} = 5 V		13.8	15	V
I_{GATE}	GATE pull-up current	Gate drive on, V_{GATE} = 0 V		-15	-10	mA
I_{GATE}	GATE pull-down current	Gate drive off V_{GATE} = 10 V	10	20		mA
V_{DD}	V_{DD} regulator output Voltage	3.3K Resistive load between V_{DD} output and AGND	5	5.75	6.5	V
I_{RSTout}	RSTout drive current	Force V_{RSTout}=1 V during fault condition	2.4	3	3.6	mA
t_{RST}	RST pulse width		200	500	1000	ns
V_{ad}	Auto-Detect threshold	Gate drive on; ramp V_{OUTsns}; monitor RST until it pulses.	-10	12	20	mV

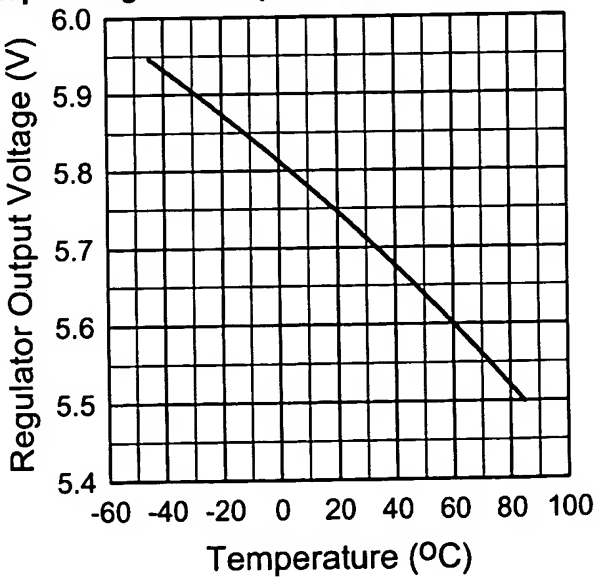
Note 1: Operating the device beyond parameters with listed "absolute maximum ratings" may cause permanent damage to the device. Typical values indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. The guaranteed specifications apply only for the test conditions listed. Exposure to absolute maximum rat d conditions for extended periods may affect device reliability.
Note2: All voltages are relative to ground unless otherwise specified.

Typical Performance Characteristics

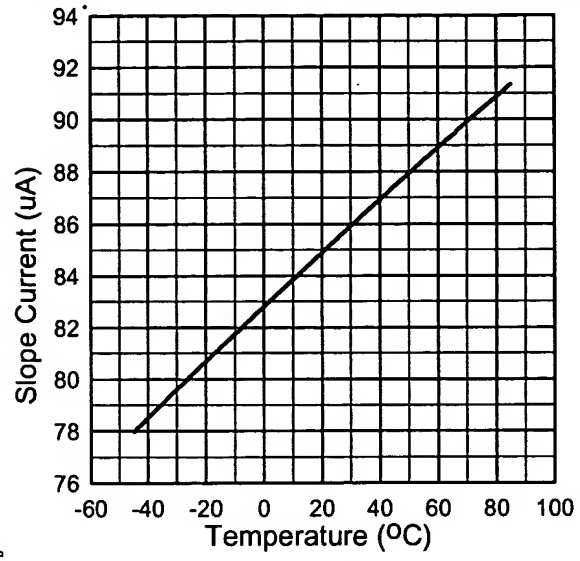
Graph 1: Icc vs. Temperature



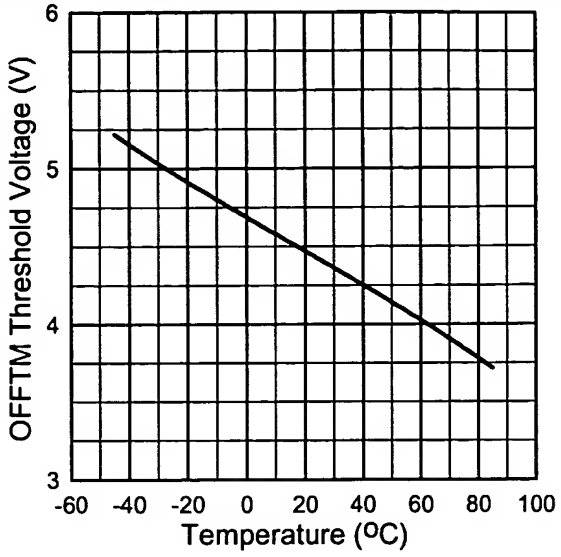
Graph 2: Regulator Output Voltage vs. Temperature



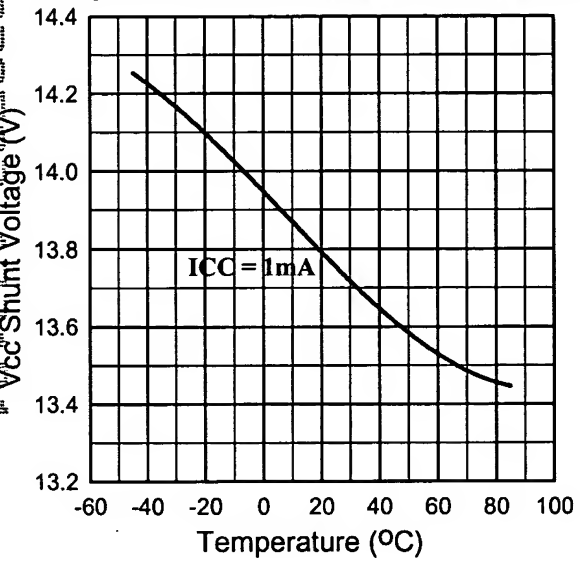
Graph 3: SLOPE Pin current vs. Temperature



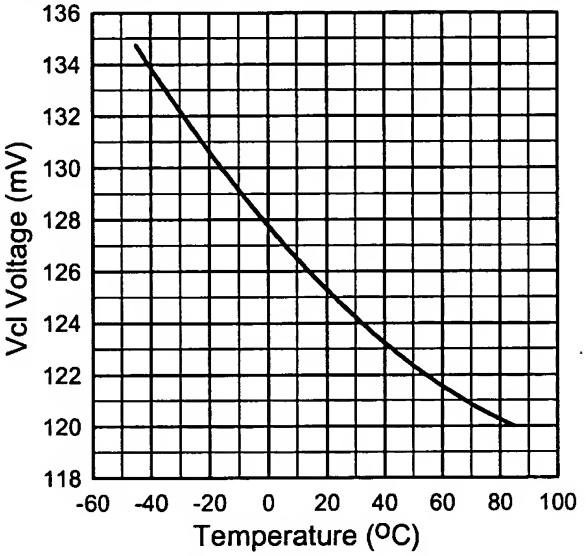
Graph 4: OFFTM Threshold Voltage vs. Temperature



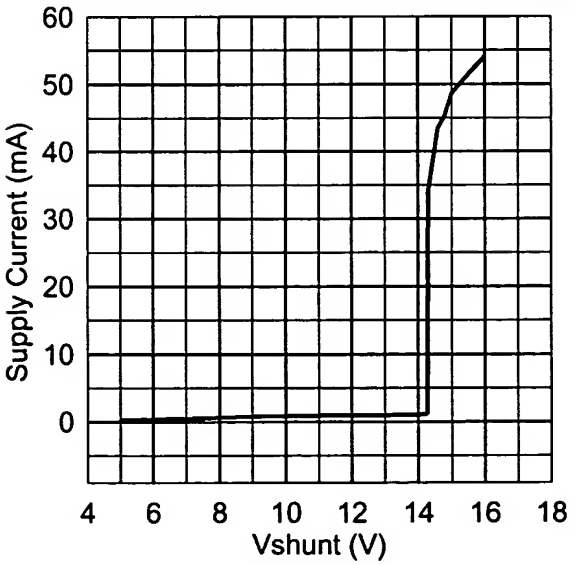
Graph 5: Vcc Shunt Voltage vs. Temperature



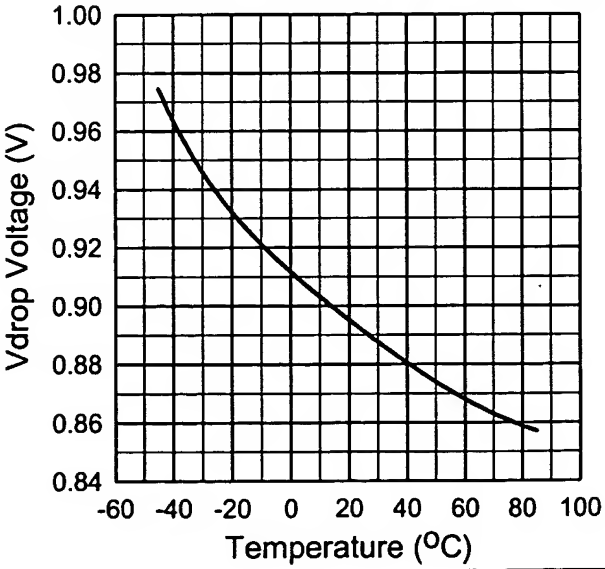
Graph 6: Overcurrent Threshold Voltage vs. Temperature



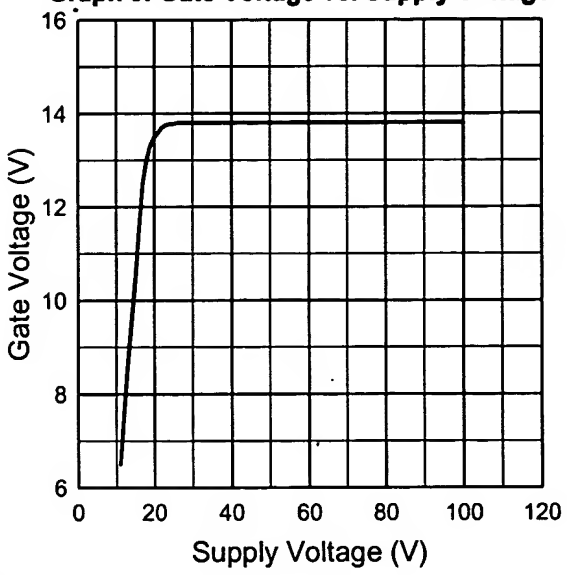
Graph 7: Supply Current vs. Shunt Voltage



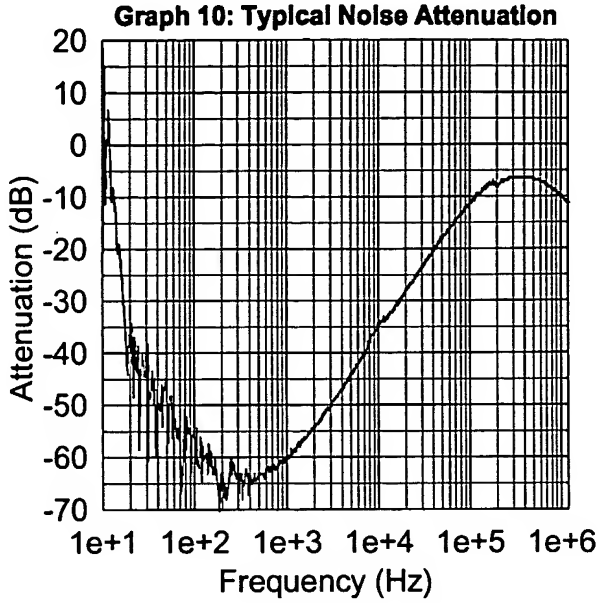
Graph 8: Vdrop Voltage vs. Temperature



Graph 9: Gate Voltage vs. Supply V ltage



Graph 10: Typical Noise Attenuation



Pin Descriptions

PIN #	SYMBOL	FUNCTION	DESCRIPTION
1	INV	Invert Input	The invert input controls GSNSin's polarity. When invert input is high compared to AGND, then GSNSin low indicates an insertion/removal event. When invert input is low, then GSNSin high indicates an insertion/removal event.
15	GSNSin	Ground Sense Input	The INV pin controls the polarity sense of this input. A 3uA internal pull-up current source causes logic high when there is no connection at this pin. With INV low or connected to AGND, a GSNSin low (or connected to AGND) will keep RSTout and GATE low, and the external power switch, Q1, off. A disconnected GSNSin pin or when Vcc is applied to it will allow normal operation
2	VCCin	Supply Voltage	Positive power-supply voltage input.
3	SHNToff	Shunt Off	This pin serves to control the enabling of the shunt circuit. When the pin is high compared to AGND, then the shunt regulator is in off position. A low level at this pin activates the shunt regulator.
4	CAPin	Active low-pass filter capacitor input	The output of the power active filter tracks this pin. Adding an external RC network matching the input noise with respect to the 3db point of the filter could reduce the noise to a minimum.
5	VDROP	Active filter offset voltage	This pin sets the drop out MOSFET voltage across the active filter.
6	SLOPE	Slope input	This input controls the current slope during power up and controls inrush currents. Adding external capacitors to this pin allow regulation and adjustment of the rate of the current slope.
7	OFFTM	Off-time	The OFFTM pin sets the delay time between power-down and restart of IXHQ100. Delay time can be increased by adding external capacitors to this pin.
8	AGND	Ground	The IXHQ100 system zero reference pin.

Pin Descriptions (continued)

PIN #	SYMBOL	FUNCTION	DESCRIPTION
9	VDDout	Regulator output voltage	Regulator output voltage provides current to drive the external circuits with respect to AGND.
10	VCL	Overcurrent threshold bias voltage	Sets the overcurrent threshold bias voltage.
11	SOURCE	Current input sensor	Input for sensing current through power device with respect to AGND.
12	GATE	Output	Control voltage for driving external MOSFET.
13	OUTsns	Out sensor signal	This signal senses the output voltage of the circuit.
14	RSTout	Output Reset	A low at this pin indicates detection of an insert/removal event or overcurrent detection.
16	NC	N/A	Not Connected

IXHQ100 Logic Diagram

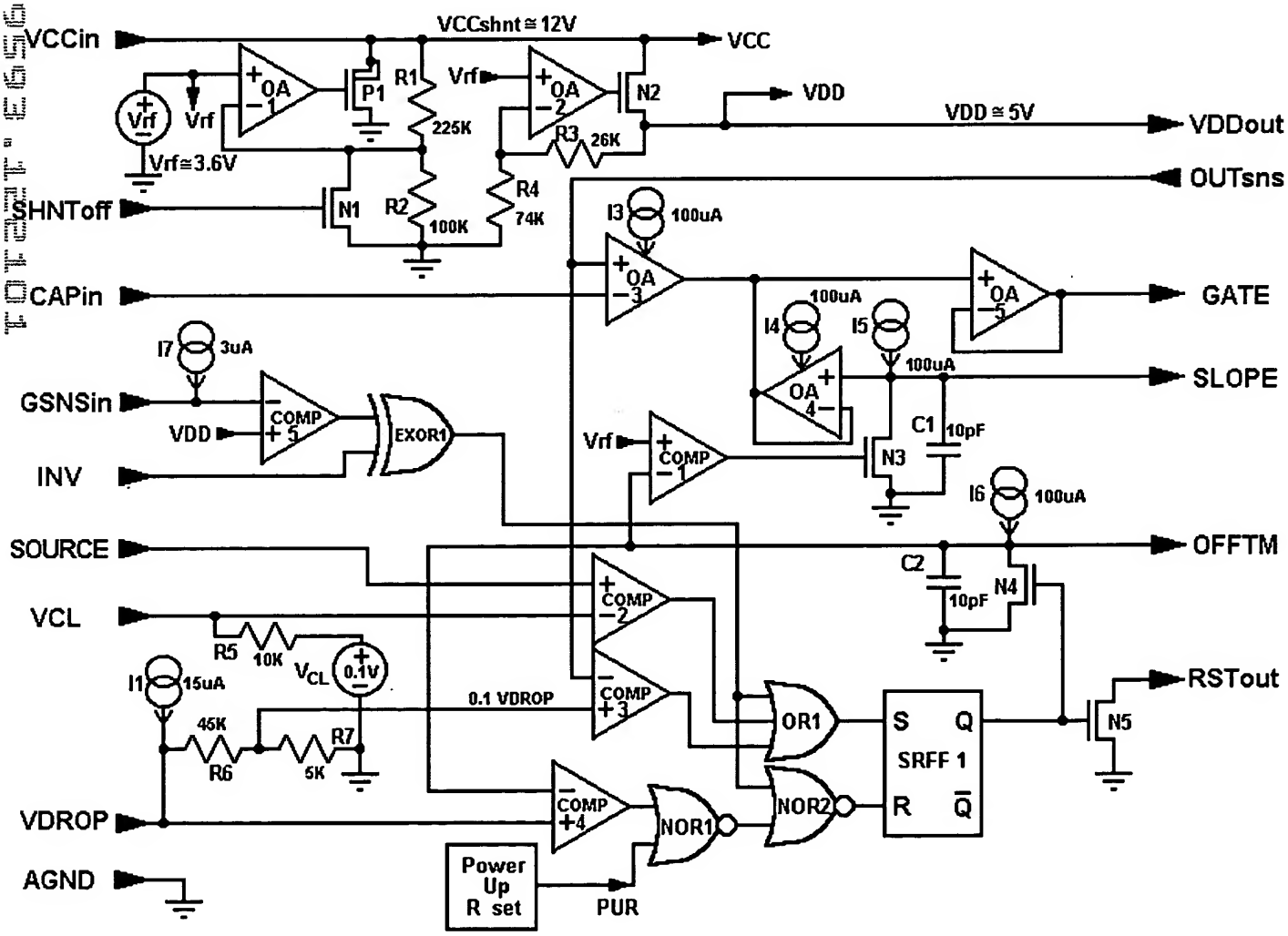


Figure 2

DEVICE OPERATION*

A hot swap operation involves removal and reinsertion of a device while the system using it remains in operation. Such an operation could cause external capacitors to draw currents high enough to disturb system operations or even cause permanent damage to both the device and the system.

The IXHQ100 is designed to prevent any disturbances or damage during such occurrences, allowing the circuit board to be safely inserted and removed from a live backplane. Capable of operating under three modes, the chip also acts as a power active noise filter and an auto-detect circuit.

Insertion Process

As the circuit board is inserted into the backplane, physical connections should be made to ground to discharge any electrostatic voltage. The insertion process begins when power and ground are supplied to the board through pins on the blackplane.

Once power is applied, the IXHQ100 starts up but does not immediately apply power to the output load. The internal Power Up Reset logic (see in Figure 2) turns on for 10 µs prior to any other logic. This pulse goes through two NOR gates and resets SRFF1 Flip Flop. Once SRFF1 is reset, the current source, I6, charges the OFFTM pin at a rate proportional to the size of the external capacitor, C7 (fig 1). During the time the OFFTM pin is ramping from 0V to Vrf (~5V), which is the $T_{off\text{-}delay}$, COMP1 keeps N3 ON so V_{SLOPE} stays at 0V. After $T_{off\text{-}delay}$, V_{OFFTM} becomes greater than Vrf, and COMP1 goes low, driving N3 to off state. I5 now starts to charge C1, ramping +ve i/p of OA4. OA4 buffers V_{SLOPE} and sets the GATE output ramp.

It is assumed that when the circuit board is first inserted into the backplane, the voltage across the external load, V_{load}, is zero. As V_{SLOPE} rises, its rate of increase determined by the value of the external capacitor, C8 (figure1), and the value of the internal current source, I5. V_{GATE}'s rate of increase follows V_{SLOPE}. As soon as V_{GATE} exceeds V_{thQ1} (figure 1) of the external power MOSFET, drain current I_{dQ1} starts to flow. The rate of increase of I_{dQ1} is proportional to the rate of increase of V_{SLOPE}, and is independent of the size of C5 , the total filter capacitance of the load. Note that this rate, which is directly proportional to C7 and inversely proportional to C8, could be adjusted . Similarly the Toff-delay can be adjusted and is directly proportional to the size of C7.

Normal Operation

With continuous $-V_{in}$ applied, the IXHQ100 acts as an active power filter by modulating the voltage drop across the external Power MOSFET V_{ds} so that any noise on $-V_{in}$ is cancelled by V_{ds}.

The direct connection of IXHQ 100's AGND pin to $-V_{in}$ allows the V_{drop} (internally set to ~750mV) to set the ~90% of the maximum peak noise voltage reject by the IXHQ100. The internal V_{drop} setting of ~750 mV allows 1.35 Vpp of noise rejection. Graph on page 5 illustrates the level of ripple attenuation during normal conditions. Notice that the noise rejection is very high (~60db) between 400Hz to 40KHz, which is optimal for most hot swap applications.

Flip-flop setting and resetting

The flip-flop, SRFF1 (fig 2), used in the IXHQ100, is reset dominant. Hence when both S and R inputs are driven high, the SRFF1 remains reset. Under normal operation, S input becomes high whenever OR1 output is high and R input is low. In turn, OR1 goes high if any one of the outputs of EXOR1, or COMP2, or COMP3 goes high.

EXOR1 output goes high if it detects the loss of either Gnd or -Vin. If INV input is connected to

*Unless otherwise stated, all symbol and device references are referred to the logic diagram (Fig 2) on page 6

Vcc, then GSNSin pin can be used to detect the presence or absence of -Vin. If INV is connected to AGND, then GSNSin pin can be used to detect the presence or absence of Gnd.

COMP2 output goes high whenever an overcurrent or a short circuit condition is detected. The inverting input to COMP2 is connected to the VCL output pin which is internally set at approximately 120mV. As shown in Figure 1, one side of R4 is in series with the source of Q1, the drain output of which drives the load connected to J8. The return side of R4 is connected to -Vin through J1. For R4 = 0.02Ω, Q1 source currents greater than 6A will turn on COMP2 and will be considered either an overcurrent or short circuit event.

COMP3 goes high whenever the voltage at OUTsns with respect to AGND becomes less than 0.1*VCL(approximately 12mV). This can only occur if either the current drawn by the driven load is less than 600mA (12mV/.02) or $-V_{IN}$ is disconnected. This Auto-Disconnect technique automatically detects load disconnections without needing additional sensors.

Thus the SRFF1 will reset when one of the following events occur:

1. Loss of AGND or -Vin.
2. Overcurrent or short circuit.
3. Auto-Disconnection

A valid S input into SRFF1 will immediately drive its output, Q1, to high and will turn on both N5 and N4. N5, an open drain output, will result in RSTout being driven low. A current limiting resistor, R1, in series with a 4N35 LED connected to V_{DD} (fig 1) can be used to generate an isolated reset pulse. Turning on N4 will discharge C7 and the internal 10pF capacitor (fig 2). As soon as V_{OFFTM} drops below V_{DROP} =~0.9V, COMP4 in Figure 2 will turn on through NOR1 and NOR2, and resets SRFF1 with a high applied to its R input. This act will then turn off both N5 and N4 and allow OFFTM pin to initiate its positive ramp as a result of I6 charging the capacitors C7 (Figure 1) and C2 (Figure 2) connected to the OFFTM pin.

Restart Operation

The IXHQ100 will automatically attempt to restart once a disconnection and reconnection is detected. Either PUR or COMP4 going high will reset SRFF1 during normal operation of the IXHQ100 (fig 2). Resetting SRFF1 turns off N4 and N5, and the OFFTM pin ramps up in response. During this ramp, as long as V_{OFFTM} is less than Vrf=~4.5V, COMP1 will keep N3 on and C1 (Figure 2) and C8 (Figure 1) discharged. After $T_{off\text{-}delay}$, V_{OFFTM} is at Vrf, COMP1 output then goes low, turning off N3. Now the SLOPE pin is free to ramp up as a result of I5 charging C1 (Figure 2) and C8 (Figure 1). The two unity-gain buffers, OA4 and OA5, reflect V_{SLOPE} at the GATE output pin during this positive ramp. As soon as V_{GATE} overcomes the V_{Q1th}, normal operation is resumed.

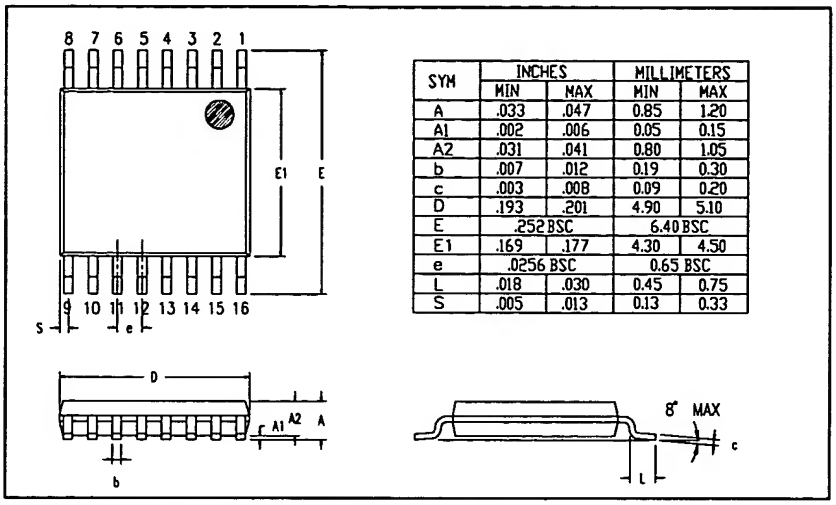
Fault Operation

When the output load current is such that the voltage drop across the current sense resistor between the SOURCE pin and the AGND exceeds VCL (internally set to ~120 mv), the GATE output is driven low to turn off the external Power MOSFET connected between the load and $-V_{in}$. An external capacitor connected between OFFTM pin and AGND pin determines the off time $T_{off\text{-}delay}$. IXHQ100 will restart the turn on sequence of the external Power MOSFET with a load voltage slope determined by the size of the external capacitor that is connected to the SLOPE pin.

Sh rt Circuit Prev nti n

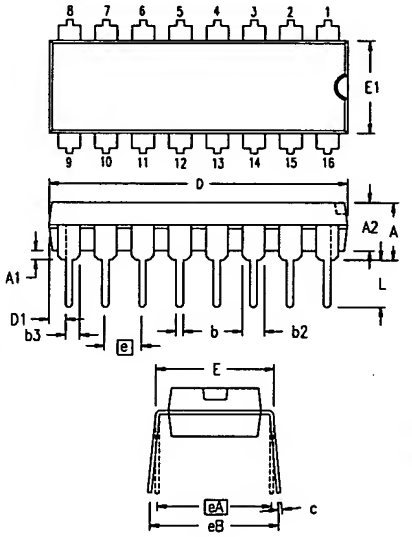
When the IXHQ100 detects a short in the load, a restart is automatically initiated. The GOUT drops to zero and waits one $T_{off\text{-}delay}$ before SLOPE ramps up. As before, normal operation is resumed.

Package Outlines: 16 PIN TSSOP



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.033	.047	0.85	1.20
A1	.002	.006	0.05	0.15
A2	.031	.041	0.80	1.05
b	.007	.012	0.19	0.30
c	.003	.008	0.09	0.20
D	.193	.201	4.90	5.10
E	.252 BSC		6.40 BSC	
E1	.169	.177	4.30	4.50
e	.0256 BSC		0.65 BSC	
L	.018	.030	0.45	0.75
S	.005	.013	0.13	0.33

Package Outlines: 16 PIN PDIP



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.140	.180	3.56	4.57
A1	.015	.040	0.38	1.02
A2	.125	.145	3.18	3.68
b	.015	.020	0.38	0.51
b2	.055	.065	1.40	1.65
b3	.035	.045	0.89	1.14
c	.009	.012	0.23	0.30
D	.745	.800	18.92	20.32
D1	.010	.040	0.25	1.02
E	.300	.325	7.62	8.26
E1	.240	.270	6.10	6.86
e	.100 BSC		2.54 BSC	
eA	.300 BSC		7.62 BSC	
eB	.300	.430	7.62	10.92
L	.120	.140	3.05	3.56

NOTE: THIS DRAWING MEETS ALL REQUIREMENT OF JEDEC OUTLINES MS-001 AB AND BB.

Ordering Information

Part Number	Package Type	Grade
IXHQ 100PI	16 PIN PDIP	Industrial
IXHQ 100SI	16 PIN TSSOP	Industrial

IXYS Corporation
3054 Bassett St; Santa Clara, CA 95054
Tel: 408-982-0700; Fax: 408-496-0670
e-mail: sales@ixys.com

IXYS Semiconducotr GmbH
Edisonstrasse15 ; D-68623; Lampertheim
Tel: +49-6206-503-0; Fax: +49-6206-503627
e-mail: marcom@ixys.de